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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,622	10/27/2000	Jyh-Ming Jong	P4928/06145.003001	4922

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,622	JONG ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE filed on 7/22/04 in which claims 1-7 and 9-13 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-6, 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bortolini et al U.S. Patent NO 5,268,635.

As per claims 1 and 9, Bortolini et al teaches discloses an apparatus for detecting a noise error of a signal comprising: an high comparator (see fig.5, element 503 and col.4, lines 18-20 and 46-50) that references a high voltage limit with the signal and generates an output; a low comparator (see fig.5, element 504 and col.4, lines 18-20 and 46-50) that references a low voltage limit with the signal and generates an output; and a circuit (see fig.5 element 505 and col.4, lines 23-25 and 47-50) that processes the high comparator output and the low comparator output, wherein at least one of the high comparator output and at least one of low comparator output clocks the circuit and wherein the circuit generates an emitting light is considered as the claimed (alarm) if a noise error is detected.

As per claim 2, the apparatus of Bortolini does include a high-to-low sub-circuit that detects a noise error during a (1)(rising) signal transition and a low-to-high sub-circuit that detects a noise error during a (0)(falling) signal transition (see col.4, lines 23-60).

As per claim 4, the apparatus of Bortolini does include a differential amplifier (see fig.5 and col.4, lines 20-22).

As per claim 5, the apparatus of Bortolini includes a sense amplifier (see col.4, lines 20-22, 45-47).

As per claims 6 and 10, the apparatus of Bortolini inherently includes high voltage limit and the low voltage limit is 300 mV.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 7, 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bortolini U.S. Patent No 5,268,635 in view of Nemetz et al U.S. patent No 5,923,191.

As per claim 3, Bortolini teaches all the features of the claimed invention including a belay buffer (see fig.5 element 507 and col.4, lines 41, 58); a flip-flop circuit (see fig.5 element 506 and col.4, line 5)

However Bortolini does not teach a plurality of flip-flop circuits and an XOR logic gate.

Nemezt et al teaches a plurality of flip-flop circuits (see figs. 5a-5b elements 52-56, 62-66 and col.8, lines 49-65) and logic gate (see figs.7A-7B elements 80, 80a and col.11, line 58-67 and col.12, lines 1-67).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nemezt into Bortolini as to generate one or more error signals for each of the detected pulse width violation by logic high and low comparators as taught by Nemezt (see col.11, lines 55-65).

As per claims 7 and 13, Bortolini et al teaches discloses an apparatus for detecting a noise error of a signal comprising: an high comparator (see fig.5, element 503 and col.4, lines 18-20 and 46-50) that references a high voltage limit with the signal and generates an output; a low comparator (see fig.5, element 504 and col.4, lines 18-20 and 46-50) that references a low voltage limit with the signal and generates an output, wherein the difference between the high voltage limit and the low voltage limit is 300 mV; and a high and low circuit and a low-to-high sub-circuit that detects a noise error during a falling signal transition (see fig.5 element 505 and col.4, lines 23-25 and 47-50) that detects a noise error during a rising and falling signals transition wherein the sub-circuit generates an emitting light is considered as the claimed (alarm) if a noise error is detected; a delay buffer (col.6, line 58); (see fig.5 element 507 and col.4, lines 41, 58); a flip-flop circuit (see fig.5 element 506 and col.4, line 5)

However Bortolini does not teach either sub-circuit comprises a plurality of flip-flop circuits and an XOR logic gate.

Nemezt teaches sub-circuit comprises a plurality of flip-flop circuits and an XOR logic gate (see figs. 5a-5b elements 52-56, 62-66 and col.8, lines 49-65) and logic gate (see figs.7A-7B elements 80, 80a and col.11, line 58-67 and col.12, lines 1-67).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nemezt into Bortolini as to generate one or more error signals for each of the detected pulse width violation by logic high and low comparators as taught by Nemezt (see col.11, lines 55-65).

As per claims 11 and 12, Bortolini teaches all the features of the claimed invention including a belay buffer (see fig.5 element 507 and col.4, lines 41, 58); a flip-flop circuit (see fig.5 element 506 and col.4, line 5)

However Bortolini does not teach sub-circuit comprises a plurality of flip-flop circuits and an XOR logic gate.

Nemezt et al teaches a sub-circuit plurality of flip-flop circuits (see figs. 5a-5b elements 52-56, 62-66 and col.8, lines 49-65) and logic gate (see figs.7A-7B elements 80, 80a and col.11, line 58-67 and col.12, lines 1-67).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nemezt into Bortolini as to generate one or more error signals for each of the detected pulse width violation by logic high and low comparators as taught by Nemezt (see col.11, lines 55-65).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu U.S. patent No 5,814,903 teaches a programmable gain for switched power control.

Fukuda U.S. Patent No 5,065,413 teaches a phase locked loop circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

9/17/04

EMMANUEL BAYARD
PRIMARY EXAMINER